IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): **Satoh, Yoshihiro**	
Serial No.: **09/981,402**	Group Art Unit: **2815**
Filed: **October 17, 2001**	Examiner: **Richards, N. D.**
Title: **Semiconductor Device and Method for Its Manufacture**	
Attorney Docket No.: N32040200W	

DECLARATION UNDER 37 C.F.R. §1.131 by ASSIGNEE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I, Takeo Fujii, representing Elpida Memory, Inc., do hereby declare and state:

1. After a diligent effort, the inventor for this patent application was not available to produce a declaration to swear behind the present reference.

2. Prior to October 12, 2000, a semiconductor device and structure on a silicon substrate as described and claimed in this patent application was conceived. Disclosure of the invention is shown in the communication dated August 9, 2000 (see Exhibits A and B).

3. On October 20, 2000 a patent application for the invention was filed in Japan, a WTO member country.

4. On October 17, 2001 this patent application, based on the Japanese Patent Application, was filed in the U.S.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby declare that all statements made herein are true and with the knowledge that willful false statements and like so made are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code.

Signed:

Takeo Fujii

Name: Takeo Fujii

Date

for **Elpida Memory, Inc.**

Executive Manager
Intellectual Property Gr.
Finance & Legal Office

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

EXHIBIT A

DISCLOSURE DOCUMENTS IN SUPPORT OF
DECLARATION UNDER 37 C.F.R. §1.131

For Serial No.: 09/981,402
Applicant(s): SATOH, Yoshihiro

アイデア提案書	事業部整理番号:
提案日:2000年 8月 9日	グループコード: 部内番号:
[承認欄]部長: 課長:	半特技受付日:

[提案者記入欄]

E-mail: y-satou@eu.jp.nec.com
提案者所属:1メモリ デバイス設計部
提案者氏名:佐藤 好弘 社員番号:

適用・応用分野:半導体装置の構造および製造方法
適用製品名: 売上規模: (百万円/年)
実験・試作状況:○実験・試作完了 ●実験・試作中 ○実験・試作予定あり ○実験・試作予定なし
先行特許調査(調査した中で近い特許公開番号):
先行文献調査(調査した中で近い公知例):
特許検索式:
関連提案・特許:
サンプル出荷/社外発表予定:●無 ○有(早い方の日:)
出願希望種別:○コンカレント ○S級 ●通常出願(

[発明相談コメント欄] センター担当: 年 月 日

[証人署名欄]

本提案書(図面を含む)の第1ページから第 ページを読んで発明内容を理解しました。
氏名: 堀場信一 2000年8月9日
[発明者署名欄]
氏名: 佐藤好弘 2000年8月9日
氏名: 20 年 月 日

整理番号: 744-10831 本文第2/4頁

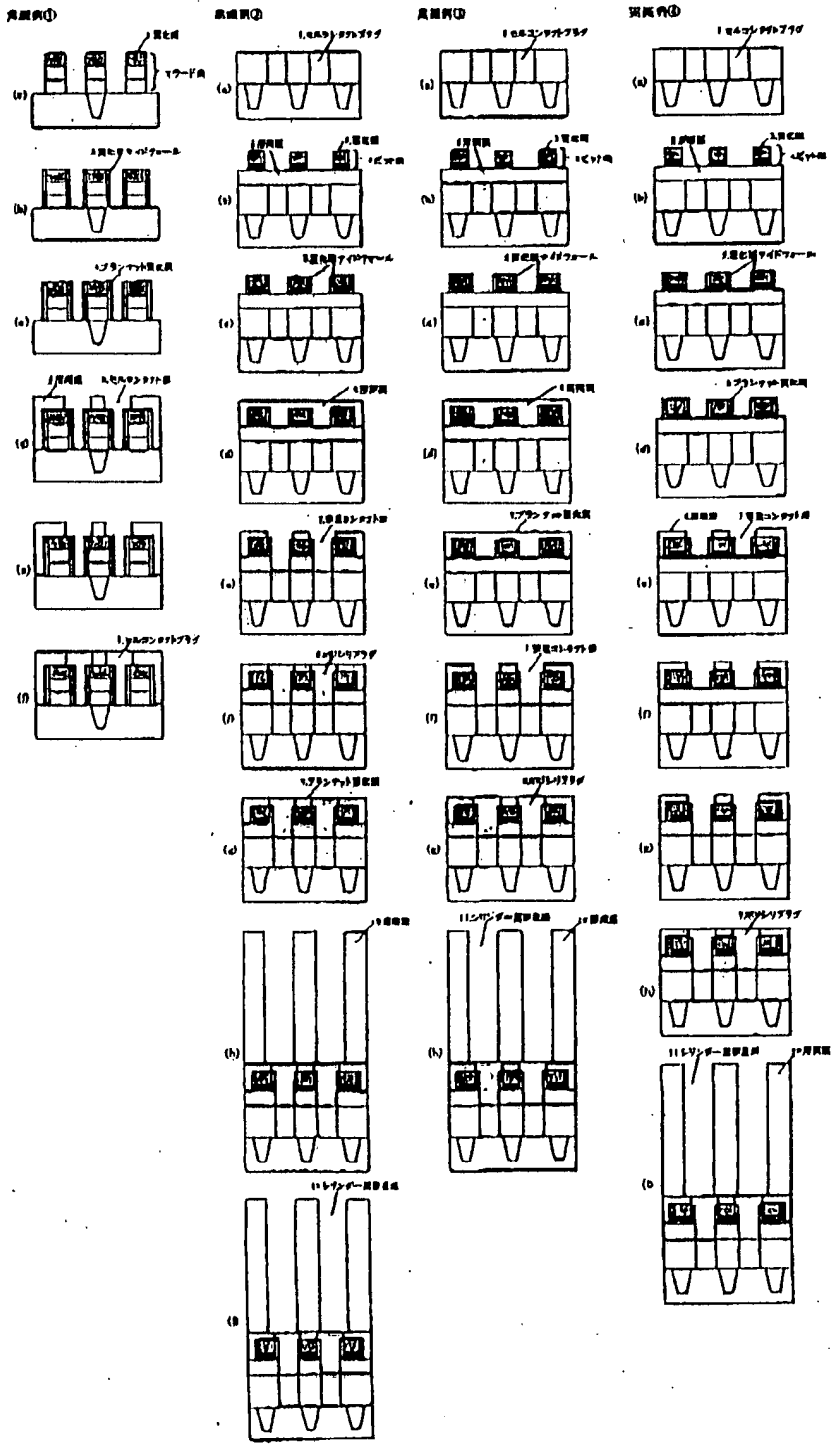
1.【発明の名称】

半導体装置の構造および製造方法

2.【発明の特徴】

容量絶縁膜にタンタルオキサイド(Ta2O5)を用いた場合のDRAMにおいて、その有機系原材料に含まれるカーボンの拡散を防止するための膜として、シリコン基板と容量絶縁膜の間に窒化膜で構成されるストッパー膜を形成する。

8. 1【発明の図】



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

EXHIBIT B

Translation of Disclosure Document of EXHIBIT A

IN SUPPORT OF DECLARATION UNDER 37 C.F.R. §1.131

For Serial No.: 09/981,402
Applicant(s): SATOH, Yoshihiro

Idea proposal	Business Unit Management Number:
Date of proposal: Aug 9, 2000	Group code: 4J600 Section Internal Number:
[Approval] Director:	Received:

[Items filled in by the proposer]
e-mail: y-satou@eu.jp.nec.com
Section where the proposer belongs: Memory Device Design 1,

Name of the proposer: Yoshihiro Sato Employee Number:
Application field: construction and manufacturing method of a semiconductor device
Applied product name: Sales amount: (million Yen/year)
Experiment/prototyping status: _ experiment/prototyping done _ experimenting/prototyping _ experiment/prototyping planned _ experiment/prototyping not planned
Preceding patent research (close Patent publication number in the research):
Preceding reference research (close known example in the research):
Patent search:
Related proposal/patent:
Sample shipment/presentation schedule outside company:

Application type requested: _ Concurrent _ S class _ Normal application

[Invention Consulting comment] Person in charge at the Center: Date:

[Witness signature]
I have read the proposal (including figures) from Page 1 to Page and understood the content of the invention.
Name: Shinichi Horiba Date: August 9, 2000
[Inventor signature]
Name: Yoshihiro Sato Date: August 9, 2000
Name: Date:

1. [Name of the invention]
Construction and manufacturing method of a semiconductor device

2. [Characteristics of the invention]
For DRAMs in which tantalum oxide (Ta2O5) is used for the capacitance insulation film, a stopper film that consists of a nitride film is formed between the silicon substrate and the capacitance insulation film to prevent the diffusion of carbon contained in the organic materials.

8.1 [Figures of the invention]